This listing of claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1-15. (cancelled).

16. (previously presented) A method for simulating a system which comprises a core in a microprocessor or in a microcontroller and peripheral modules connected to the core, the method comprising:

executing a first series of method steps for simulating the system using predetermined signal patterns; and

executing a second series of method steps by the core of the microprocessor or of the microcontroller only in order to request and evaluate system states brought about by the execution of the first series of method steps, the execution of the first series of method stops being interrupted by the execution of the second series of method steps as stipulated by markers inserted into the first series of method steps, the second series of method steps being executed in an accelerated operating mode which is matched to the evaluation.

17. (previously presented) The method according to claim 16, wherein the first series of method steps is executed such that the core and the peripheral modules are simulated on a clock cycle basis.

18. (previously presented) The method according to claim 17, wherein the first series of method steps is a succession of successive program codes.

19. (previously presented) The method according to claim 18, wherein the markers are formed by opcodes or opcode sequences which are normally not used in the program code.

20. (previously presented) The method according to claim 18, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

21. (previously presented) The method according to claim 16, wherein the first series of method steps is a succession of successive program codes.

22. (previously presented) The method according to claim 21, wherein the markers are formed by opcodes or opcode sequences which are normally not used in the program code.

23. (previously presented) The method according to claim 22, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

24. (currently amended) The method according to claim 16 ~~22~~, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

25. (previously presented) The method according to claim 21, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

26. (previously presented) The method according to claim 17, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

27. (previously presented) The method according to claim 16, wherein, during the second series of method steps, prescribed peripheral modules have their functions simulated at the same time.

28. (previously presented) An apparatus for simulating a system which comprises a core in a microprocessor or in a microcontroller and peripheral modules connected to the core, in which the system executes a first series of method steps for simulating the system using predetermined signal patterns; and executes a second series of method steps by the core of the microprocessor or of the microcontroller in order to request and evaluate system states brought about by the execution of the first series of method steps, the execution of the first series of method stops being interrupted by the execution of the second series of method steps as stipulated by markers inserted into the first series of method steps, the second series of method steps being executed in an accelerated operating mode which is matched to the evaluation; the apparatus comprising:

a control unit for simulating the system by producing signal patterns which fundamentally have clock cycle accuracy and for requesting and for evaluating the system states brought about by the simulation during a program interruption by activating an instruction set simulator.